Area & power Efficient Router in 2-D Mesh Network-on-Chip Synthesis Results

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Abstract – Network on Chip (NoC) is the solution to the system design which have offer us bulk circuit. Here we are minimizing the size of the circuit to great extent. NoC also has the positive aspect to optimize the area along with power. In this proposed project we are focusing on optimization of area, power, and throughput and to have adaptive interface through wishbone. NoC enables us to have and communication with IPs or different nodes through various packet switching algorithm. The complex SoC designs are made more efficient and less complex with the simple NoC.

Index Terms – Area, Power, Throughput.

1. INTRODUCTION

The technology is improving and so the number of IP's on a chip are increasing this is resulting in degradation of the performance, area and the power. In addition to this one more challenge is communication between the IP cores. On Chip Network is a new paradigm to overcome the system on chip communication challenges. NoC uses the different routing algorithms and flow control technique to overcome the networking problem faced in previous on chip network architecture. NoC being a communication solution it will deal with the data packets. Many number of data packet transmission will take place when implemented on real time, this will give rise to packet encryption and decryption chaos at transmitter and receiver. This can be avoided by initializing the priority encoder along with arbiter.

The use of crossbar switch will also prove beneficial as the internal switch bandwidth is increased, and the allocation according to the priority of packet is done. Arbiter are used to match N request to 1 resource. The Arbiters play a crucial role in the implementation of pended and split-transaction buses. These are the so-called since they grant a requested resource (the shared bus) only to one of the requester. Network adapters are the interfacing peripheral between IP cores and the routers. The desired signal is converted to packet and then transmitted through the channel at the receiver end, these signals are converted back to original format from the packets. At routers the packets are routed to suitable output channel or forwarded back to the buffers. In the NOC design, the two FIFO queues are needed. One register is for the network output channel, thereby being called network output channel buffer.

2. REVIEW ON LITERATURE

A round-robin token passing bus or switch arbiter guarantees Fairness (no starvation) among masters and allows any unused timeslot to be allocated to a master whose round-robin turn is later but who is ready now [13]. Networks-on-Chip delivers more number of scalable communication resources to overcome the limitations of bus interconnects. V.Soteriou stated that by increasing crossbar switches and arbitration schemes, the throughput of the Network on Chip router can be increased. The idea of inserting repeater by eliminating some of the buffers on inter-router links with adaptive control router [1]. Ying-Cherng Lan introduced the increased buffer utilization within the chip by making the channels bi-directional. Dynamically configuring the channel direction of the router and sharing the channel. Due to double crossbar design and control logic there is a 40% area overhead over the typical NoC router architecture. Lee introduced a wired/wireless design called Hybrid WCube that each group of 64 nodes within the chip uses a centralized wireless hub. Ganguly proposed a scalable hybrid design using several centralized wireless hubs with ring topology. Chifeng Wang proposed a NOC architecture where signal carrying interconnects within the chip will be bottle neck to enhance the performance of the system and the reliability. Power reduction proposed by eliminating the cross talk coupling effect and reducing the self-switching[15].

3. PROPOSED METHOD

3.1. Router

Routers have five sets of channels connected to it. As the Mesh organization is used in the network, we can identify four directions: north, east, south, west and one additional channel going to the local network adapter. The architecture consists of the boundary layer that holds and manages the input signals and buffers and internal layer where the packets are routed to the suitable output channel or forwarded back to the buffers. Each input channel and output channel has its own decoding logic to

increase the performance of the router to store the data for a short time span buffers are recommended at respective ports. The store and forward method is used here for data transmission. Control logic duty is to make decisions to grant access to a port request. In this way communication is established between input and output ports. The communication between the source and destination is called packet switching mechanism.

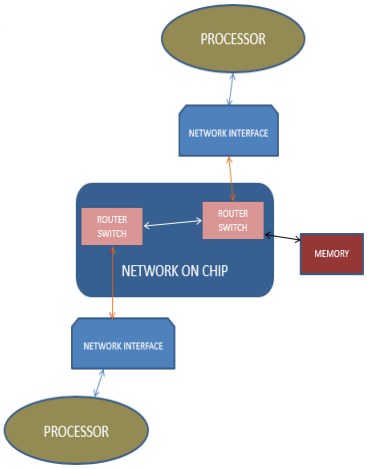


Figure 1. Block dig of NOC

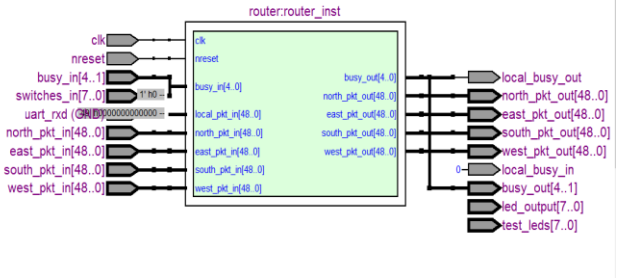


Figure 2. RTL View of Router

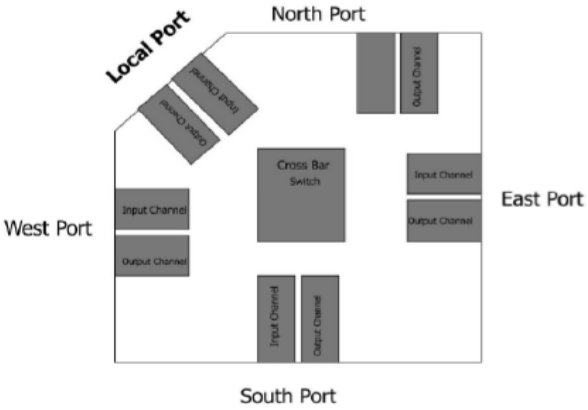


Figure 3. Block diagram of Mesh based router

3.2. NETWORK ADAPTERS

The network adapters are the interface between the IP core and the router. Network adapter purpose is to convert signals from the local bus into a packet format suitable for the network and back again. There are two types of network adapters master and slave. The master network adapter receives the following signals from the master device: write Address, write enable, write data and read request. A master Device can connect to the network adapter and the network should be totally transparent. The NA sends back not ready, Read return and read data. Any device wishing to connect to

The network will have to handle the not ready signal from the network adapter. Network adapter's output interfacing that with a router is a packet out. It can receive the busy signal from the router and a read return packet.

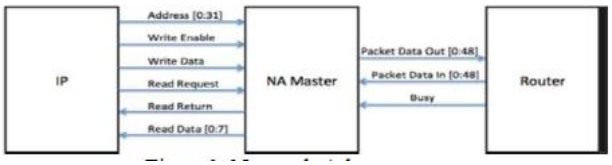


Figure 4. Network Adapter

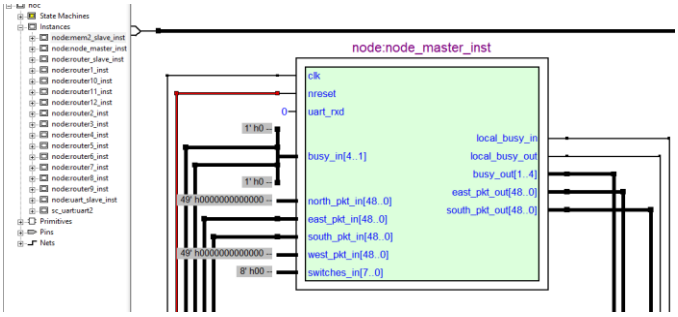


Figure 5. RTL View of Master

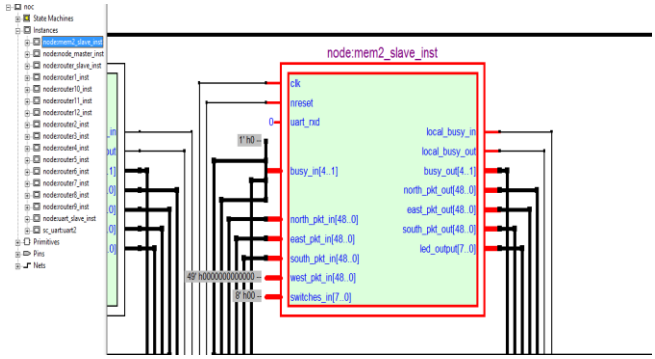


Figure 6. RTL View of Slave

3.3. FIFO

FIFO (first in initial out) is employed as input buffer as

temporary knowledge storage. The standing of FIFO decides the communication will begin or not. If the FIFO is empty the information will be written in it and communication will begin. If FIFO is full, data will be browse or will be forwarded to its destination router. Within the router Grant /acknowledgement signals square measure won't to access the FIFO .The browse and write operation of FIFO are managed by FSM. FSM controls the browse and write operation of FIFO per its standing. If FIFO is empty and having house to store, then FSM can generate a proof in relevancy the request returning to input channel and thus the write operation starts. If FIFO is full or not having house to store the information, the write operation s stops and also the acknowledgement signal goes low. The browse and write operation of FIFO is controlled by FSM. FSM controls the browse and write operation of FIFO per its standing. If FIFO is empty, FSM can provide acknowledgement signal with relevancy the request sent by the input channel of the router.

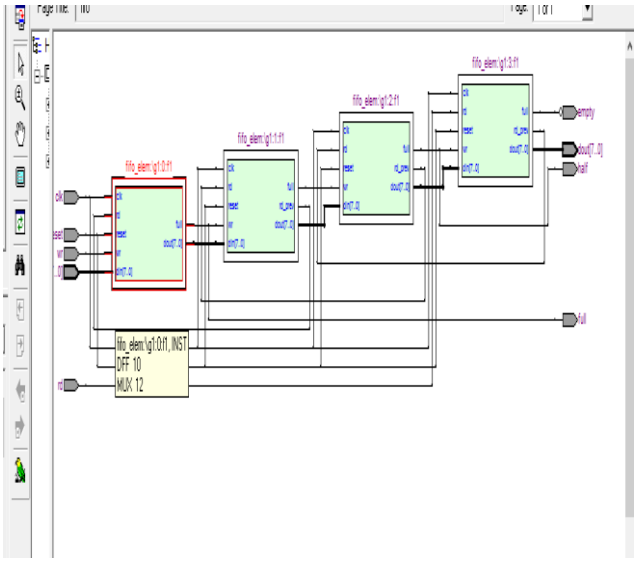


Figure 7. RTL view of FIFO

3.4. WISHBONE

The wishbone System-on-Chip (SoC)/Network-on-chip (NoC) Interconnection Architecture for Portable IP Cores is a flexible design methodology for use with semiconductor IP cores. Its purpose is to stimulate design reuse by alleviating System-on-Chip integration problems. This is accomplished by creating a common interface between IP cores. It defines that the standard data exchange between IP core modules is to create an portable interface that is independent of the underlying semiconductor technology. For example, WISHBONE interconnections can be made so that they will support both FPGA and ASIC target devices. Thus to implement this NoC design on FPGA wishbone is acting like a interfacing protocol.

4. EXPERIMENTAL RESULTS

1) *Area Synthesis Result*

Flow Status	Successful - Sun Jun 19 12:12:31 2016
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	NOC
Top-level Entity Name	noc
Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	13,586 / 68,416 (20 %)
Total combinational functions	12,352 / 68,416 (18 %)
Dedicated logic registers	7,596 / 68,416 (11 %)
Total registers	7596
Total pins	36 / 622 (6 %)
Total virtual pins	0
Total memory bits	256 / 1,152,000 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

2) *Power synthesis results*

PowerPlay Power Analyzer Status	Successful - Sat Jul 02 13:19:09 2016
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	NOC
Top-level Entity Name	noc
Family	Cyclone II
Device	EP2C70F896C6
Power Models	Final
Total Thermal Power Dissipation	197.56 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	154.96 mW
I/O Thermal Power Dissipation	42.60 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

3) *Throughput*

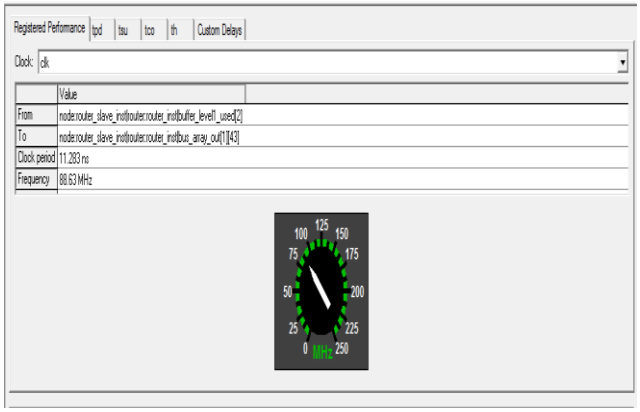
Throughput = No. of bits processed * Clk Frequency/ No. of Clk Cycles per output

=49*88.63 MHz/2

=2 Gbits/s

4) *Operating Frequency*

Operating Frequency= 88.63MHz.



5. CONCLUSION

By using the VHDL we were able to carry out synthesis and RTL of the NoC. The VHDL implementation is performed on the Altera DE2 board using Quartas 8.2 and the results of RTL along with synthesis are obtained. The ultimate goal of optimization of the area overhead of NoC, reduction in power dissipation and high throughput can be verified from the results obtained. After successful implementation we have obtained the results of 2GB/Sec, operating frequency of 88.63Mz, 13,586 Logic Elements used thus area overhead can be calculated and total thermal power dissipation of 197.56 mW was achieved. The compatibility of this designed was tested by implementing on FPGA Altera DE2 board of cyclone2 series through the wishbone interfacing.

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